UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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			EXAMINER
25920	7590	10/19/2004	NGUYEN, STEVEN H D

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ART UNIT	PAPER NUMBER
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	09/780,054	PARRUCK ET AL.
	Examiner	Art Unit	
	Steven HD Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _09 February 2001_ .

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1 and 7-28_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) _28_ is/are allowed.

6) ☒ Claim(s) _1,7-23,26 and 27_ is/are rejected.

7) ☒ Claim(s) _24 and 25_ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

    If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____ .

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

    a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____ .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1.   The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2.   Claims 9-10 and 27 are rejected under 35 U.S.C. 112, second paragraph, as being

indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention.

As claim 9, "said virtual connections" is vague and indefinite because it does not refer to

any previous elements.

As claim 27, "the output arbitrating structure" is vague and indefinite because it does not

refer to any previous elements.

There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5.   Claims 1 and 7-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gun

(USP 5777984) in view of Caldara (USP 5748629) and McClure (USP 5790770).

Regarding claims 1 and 7-16, Gun discloses (Figs 1-15 and col. 1, line 15 to col. 24, line

14) a data switch for communicating among a plurality of devices coupled to said data switch in

a digital data network wherein a virtual connection is represented by a connection between a first

device of said plurality of devices and a second device of said plurality of devices of said digital

data network, said switch including a switch element having a switch matrix (Fig 5, Ref 154); at

least one input switch access port structure coupled to said switch matrix containing a plurality

of input back pressure buffer structures wherein said plurality of input back pressure buffer

structures is configured to allow input back pressuring to be accomplished on a per-virtual

connection basis (Figs 6-7, Ref 141 and Fig 5 or 8, Ref 140 which includes a plurality of per VC

queue and feedback for generating a feedback signal to the source that is transmitting the data

cell to the switch 154); a plurality of input ports (Fig 5, Ref 160) coupled to said at least one

input switch access port structure (Fig 5, Ref 140) wherein said plurality of input ports are

coupled to a plurality of traffic generators (Fig 4, Ref 102); a size of said plurality of input back

pressure buffer structures are individually set (Fig 8, Ref 290); a size of a single input back

pressure buffer structure of said plurality of input back pressure buffer structures is optimized by

specifying a threshold window which includes a maximum and minimum size for said input back

pressure buffer structure (Local Threshold is maximum and minimum is zero; See col. 11, lines

5-67); a size of said plurality of input back pressure buffer structures is configured for a plurality

of said virtual connections (col. 11, lines 5-67 and Fig 8, Ref 290). However, Gun fails to

disclose at least one output arbitration structure coupled to said switch matrix and coupled to said

plurality of output ports wherein said at least one output arbitration device represents the

circuitry for arbitrating access to a single output port of said plurality of output ports; and a

plurality output ports coupled to said output arbitration portion wherein said pluralities of output

ports are coupled to a plurality of output destinations. In the same field of endeavor, Caldara

discloses (Figs 1-11 and col. 1, lines 15 to col. 13, lines 67) a switch comprising at least one

output arbitration structure (Fig 1, Ref 12) coupled to said switch matrix (Fig 1, Ref 13) and

coupled to said plurality of output ports (Fig 1, Ref 22) wherein said at least one output

arbitration device (Fig 1, Ref 13) represents the circuitry for arbitrating access to a single output

port of said plurality of output ports; and a plurality output ports coupled to said output

arbitration portion wherein said pluralities of output ports are coupled to a plurality of output

destinations (Col. 4, lines 60 to col. 5, lines 42); each output arbitration structure of said at least

one output arbitration structure includes a plurality of schedulers and a plurality of selectors (Fig

6, Ref VBR, ABR and UBR schedulers has a first selector for selecting one of the schedulers and

scheduler for preferred list wherein the selector are coupled to the first selector and second

selector for outputting the cell onto the link); each scheduler of said plurality of schedulers is

configured to schedule ATM cells on one of a per-virtual connection basis, a per-port basis, a per

traffic class, a per priority basis, a per group of virtual connections basis, and a cells similarly

grouped basis (Fig 6, Ref VBR, ABR and UBR schedulers; arbitration is performed on a per

virtual connection basis wherein said each scheduler of said plurality of schedulers are coupled

to connections having a same priority for switching (Fig 6, Ref VBR, ABR and UBR schedulers based on priority such as ABR, VBR and UBR); each scheduler of said plurality of schedulers is coupled to at least two buffer structures having a same priority (Fig 6, Ref VBR, ABR and UBR schedulers wherein the queues store the same priority cell such as ABR, VBR and UBR); each selector of said plurality of selectors is configured to select ATM cells using at least one of a round-robin selection technique and a weighted round-robin technique and said at least one output arbitration structure includes one of said plurality of selectors for every ATM output (col. 13, lines 46-52). However, Gun and Caldara fail to disclose an input backpressure between the switches. In the same field of endeavor, McClure discloses a switch comprising a switch fabric and plurality of input and out port, wherein each contains a queue which includes a plurality of per VC queues (Col. 2, lines 10-46, col. 4, lines 44-60 and col. 6, lines 10-20) and plurality of input back pressure buffer structures are configured for said plurality of virtual connections having a same priority (Col. 6, lines 10-20).

Since, Gun suggests feedback method at the input queue and Caldara suggests a method and system for feedback between the input and output buffer. Therefore, Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a feedback at input per queue as disclosed by McClure's method and system into Caldara's method and system which discloses a arbitration structure comprising a plurality of schedulers and selectors into the method and system of Gun. The motivation would have been to prevent a data loss and improve the throughput of the system.

Regarding claims 17-20, Gun discloses (Figs 1-15 and col. 1, line 15 to col. 24, line 14) a data switch for communicating among a plurality of devices coupled to said data switch in a

digital data network wherein a virtual connection is represented by a connection between a first

device of said plurality of devices and a second device of said plurality of devices of said digital

data network, said switch including: a switch element having a switch matrix (Fig 5, Ref 154); at

least one input switch access port structure coupled to said switch matrix containing a plurality

of input back pressure buffer structures, wherein said plurality of input back pressure buffer

structures is configured to allow input back pressuring to be accomplished on a per-virtual

connection basis (Figs 6-7, Ref 141 and Fig 5 or 8, Ref 140 which includes a plurality of per VC

queue and feedback for generating a feedback signal to the source that is transmitting the data

cell to the switch 154); a plurality of input ports coupled to said at least one input switch access

port structure, wherein said plurality of input ports are coupled to a plurality of traffic generators

(Fig 5, Ref 141 are coupled to the Ref 160 for receiving data from the sources); and at least one

output switch access structure coupled to said switch matrix, and at least one output port coupled

to said at least one output switch access structure, wherein said at least one output port is coupled

to a plurality of output destinations (Fig 5, Ref 142 for coupling to the switch and the output

ports which couples to the destination); a size of said plurality of input back pressure buffer

structures are individually set (Fig 8, Ref 290); a size of a single input back pressure buffer

structure of said plurality of input back pressure buffer structures is optimized by specifying a

threshold window which includes a maximum and minimum size for said input back pressure

buffer structure (Local Threshold is maximum and minimum is zero; See col. 11, lines 5-67).

However, Gun fails to disclose said at least one output switch access structure including, a

plurality of schedulers, an at least one selector, an at least one switch matrix output port;

arbitrates access to a respective said at least one output port. In the same field of endeavor,

Caldara discloses (Figs 1-11 and col. 1, lines 15 to col. 13, lines 67) at least one output switch

access structure (Fig 1, Ref 22) including, a plurality of schedulers (Fig 6, Ref FSPP includes a

plurality of schedulers "queue", an at least one selector (Fig 6, FSPP includes a selector for

selecting the cell from the schedulers), an at least one switch matrix output port; arbitrates access

to a respective said at least one output port (Fig 1, Ref 12 has an output port to the switch and

selecting a output port for transferring the data from the input to the output ports). However, Gun

and Caldara fails to disclose an input back pressure between the switches. In the same field of

endeavor, McClure discloses a switch comprising a switch fabric and plurality of input and out

port, wherein each contains a queue which includes a plurality of per VC queues (Col. 2, lines

10-46, col. 4, lines 44-60 and col. 6, lines 10-20) and plurality of input back pressure buffer

structures are configured for said plurality of virtual connections having a same priority (Col. 6,

lines 10-20).

Since, Gun suggests feedback method at the input queue and Caldara suggests a method

and system for feedback between the input and output buffer. Therefore, Therefore, it would

have been obvious to one of ordinary skill in the art at the time of the invention was made to

apply a feedback at input per queue as disclosed by McClure's method and system into Caldara's

method and system which discloses a arbitration structure comprising a plurality of schedulers

and selectors into the method and system of Gun. The motivation would have been to prevent a

data loss and improve the throughput of the system.

6.   Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gun, McClure

and Caldara as applied to claim 17 above, and further in view of Chiussi (USP 5689500).

Regarding claim 21, Gun, McClure and Caldara fail to discloses said at least one output arbitration device schedules cells inputted into said input ports in accordance to a weight accorded to each cell of said plurality of cells. In the same field of endeavor, Chiussi discloses a packet scheduler for scheduling the packets based on the weight (col. 12, lines 32-39).

Since, Gun, McClure and Caldara suggest the enqueued cell must be scheduled to transfer onto an output link and Caldara suggests round robin scheduling method. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to apply a weight round robin as disclosed by Chiussi's method and system into the system and method of Gun, McClure and Caldara. The motivation would have been to improve the throughput of the system.

7.   Claims 22-23 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuboi (USP 5140582).

Regarding claims 22 and 26, Tsuboi discloses (Figs 1-37 and col. 1, lines 5 to col. 38, lines 28) switch element (Fig 3) comprising an input routing portion including a switch matrix input port for receiving data (Fig 3, Ref 21); a buffer portion including a plurality of buffers (Fig 3, Ref 1411 and 1412); a switch matrix portion for routing data out from the plurality of buffers (Fig 3, The cross points); a plurality of schedulers for receiving the data from the plurality of buffers through the switch matrix (Fig 3, Ref 21 and 22); a selector (Fig 3, Ref 181 for receiving a data from the schedulers and selecting a output port for transferring packet between the buffers and output port) for receiving data from the plurality of schedulers, the selector enabling output from the switch element through a switch matrix output port. However, Tsuboi fails to disclose the schedulers receive data via a switch. However, it would have been obvious to one of

ordinary skill in the art to apply a bus into a switch for establishing a link between the devices

via a switch matrix. The motivation would have been to provide a neatly device.

Regarding claims 23 and 27, Tsuboi fails to disclose an additional input routing portion

including an additional switch matrix input port for receiving data; an additional buffer portion

including an additional plurality of buffers, the switch matrix portion routing data out from the

additional plurality of buffers; an additional output arbitrating portion, including an additional

plurality of schedulers for receiving the data from the additional plurality of buffers through the

additional switch matrix, and an additional selector for receiving data from the additional

plurality of schedulers, the additional selector enabling output from the switch element through

an additional switch matrix output port. However, it would have been obvious to one of ordinary

skill in the art to cascade a plurality of switch to form a multistage switches or form a network.

Allowable Subject Matter

1.   Claim 28 allowed.

2.   Claims 24-25 objected to as being dependent upon a rejected base claim, but would be

allowable if rewritten in independent form including all of the limitations of the base claim and

any intervening claims.

As claims 24-25 and 28, the prior arts fail to disclose a switch element, comprising: a first

input routing portion including a first switch matrix input port for receiving data; a first buffer

portion including a first plurality of buffers; a switch matrix portion for routing data out from the

first plurality of buffers and a second plurality of buffers; a first output arbitrating portion,

including, a first plurality of schedulers for receiving the data from the first plurality of buffers

and the second plurality of buffers through the switch matrix, a first selector for receiving data

from the first plurality of schedulers, the first selector enabling output from the switch element

through a first switch matrix output port; a second input routing portion including a second

switch matrix input port for receiving data; a second buffer portion including the second plurality

of buffers; a second output arbitrating portion, including, a second plurality of schedulers for

receiving the data from the first plurality of buffers and the second plurality of buffers through

the switch matrix, a second selector for receiving data from the second plurality of schedulers,

the second selector enabling output from the switch element through a second switch matrix

output port; a plurality of traffic generators for inputting data into the first input routing portion

and the second input routing portion; and a plurality of traffic acceptors to receive data from the

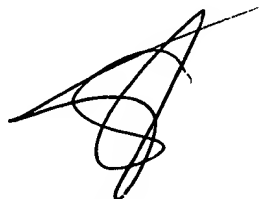first output arbitrating portion and the second output arbitrating portion.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Steven HD Nguyen whose telephone number is (571) 272-3159.

The examiner can normally be reached on 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Huy D Vu can be reached on (571) 272-3155. The fax phone number for the

organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steven HD Nguyen
Primary Examiner
Art Unit 2665
10/14/04